

Sub B2

What is Claimed is:

- [c1] A field effect transistor comprising
a ~~conduction channel of sub-lithographic width,~~
~~source and drain regions having silicide sidewalls on a surface thereof, and~~
~~polysilicon gate regions on opposing sides of said conduction channel, said polysilicon~~
~~having silicide sidewalls formed thereon and recessed from said source and drain regions.~~
- [c2] A field effect transistor as recited in claim 1, wherein said silicide sidewalls are in the form of a liner.
- [c3] A field effect transistor as recited in claim 1, wherein said polysilicon regions are connected by a connector.
- [c4] A field effect transistor as recited in claim 3, wherein said connector is a damascene connector.
- [c5] A field effect transistor as recited in claim 4, wherein said damascene conductor is formed in a trench in at least one of an isolation structure or a pad material extending over an edge of said polysilicon gate regions.
- [c6] A field effect transistor as recited in claim 1, wherein said silicide sidewalls are connected by a connector.
- [c7] A field effect resistor as recited in claim 6, wherein said connector is a Damascene connector.
- [c8] A field effect transistor as recited in claim 7, wherein said damascene conductor is formed in a trench in at least one of an isolation structure or a pad material extending over an edge of said polysilicon gate regions.
- [c9] A method of forming a field effect transistor including steps of
depositing regions of pad nitride on a silicon layer,
etching said silicon layer to undercut said pad nitride to form a conduction channel between a source region and a drain region,
depositing polysilicon where said silicon has been etched,
etching through said polysilicon,
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depositing silicide on remaining polysilicon and silicon, and
removing said silicide and polysilicon from sides of said conduction channel near said
source and drain regions.

- [c10] A method as recited in claim 9, wherein said steps of depositing said silicide and removing
said silicide define said active area of said transistor.
- [c11] A method as recited in claim 10, wherein said step of depositing silicide includes the
further step of
depositing a disposable hard mask to define said active area of said transistor.
- [c12] A method as recited in claim 11, wherein said disposable hard mask is borosilicate glass.
- [c13] A method as recited in claim 11, wherein said disposable hard mask is a doped glass.
- [c14] A method as recited in claim 11, wherein said disposable hard mask is an arsenic doped
glass.
- [c15] A method as recited in claim 11, wherein said disposable hard mask is a ozone TEOS.
- [c16] A method as recited in claim 11, including the further steps of
stripping said disposable hard mask,
depositing a conformal layer of polysilicon and silicide,
applying a further mask, and
etching silicide and polysilicon in accordance with said further mask.
- [c17] A method as recited in claim 16 wherein said silicide of said conformal layer are silicides
of tungsten, cobalt or titanium.

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